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DISTRIBUTED ARITHMETIC AND MULTIPLEXING IN A SECOND-ORDER STATE-SPACE DIGITAL FILTER

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Abstract. Two new realizations of a second-order state-space digital filter using distributed arithmetic and multiplexing are proposed. Each realization contains only one accumulator.

In state-space digital filters it is possible to eliminate overflow oscillations for any pole locations of a transfer function and simultaneously to achieve low coefficient sensitivity and optimum roundoff noise behaviors [1]. Use parallel or cascade forms on base second-order state-space sections permits to reduce the number of multipliers. However, the state-space section contains nine multipliers instead of the five which are required in a direct form section. A hardware realization of the state-space sections can be simplified by use of a distributed arithmetic. White [2,3] has offered the appropriate realization which contains three accumulators and one ROM. In the given paper two other realizations, including only one accumulator and one ROM, are presented. The effect is received by multiplexing.

The state-space section is described by the following difference equation system

$$\begin{aligned} x'_{n+1} &= a_1 x'_n + a_2 x''_n + b_1 u_n \\ x''_{n+1} &= a_3 x'_n + a_4 x''_n + b_2 u_n \\ y_n &= c_1 x'_n + c_2 x''_n + d u_n, \end{aligned} \qquad (1)$$

where u_n and y_n are the input and output variables, x'_n and x''_n are the state variables, a_j, b_j, c_j and d are coefficients.

The appropriate structure of the section is indicated on fig.1a.

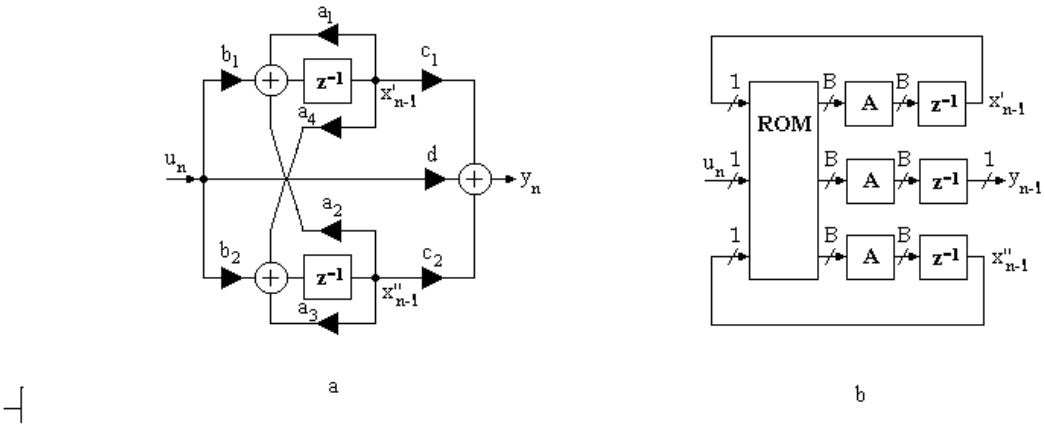

Fig.1. Structure of state-space section a) and its distributed arithmetic realization [2,3] b).

As can be seen it is necessary to execute three sums of products. The realization of this section with distributed arithmetic requires three ROM's each organized as 8 words on B bits, and three B-bit accumulators. Here for simplicity as well as in [2,3] it is accepted that wordlengths of the variables, ROM and accumulator are identical, though actually they can be essentially

distinguished [4]. According to (1) all sums of products are executed for same variables, therefore instead of three ROM's it is possible to use the one, but with organization of 8 words on 3B bits [2,3], as shown in Fig.1b. Here the block A is the accumulator. The introduction of the additional logic circuits permits to reduce the number of words in ROM up to 4 [3]. Because of bit- by-bit processing for calculation of one output sample it is required B clock periods. The processing several bits at a time increases speed but results to growth of the ROM size or to increase the number of ROM's and necessity of use of additional adders [2,3].

We shall consider now an equation

$$v_k = \beta_{0,k} w_k + \sum_{i=1}^{5} \beta_{i,k} v_{k-i}. \qquad (2)$$

Let the periodically varied coefficients $\beta_{i,k}$, i=0...5, k=0,1,2,... are connected to coefficients of the system (1) according to Table 1 and $\beta_{i,k+3} = \beta_{i,k}$, and $w_k = u_n$ at k=0, 1 and 2, $w_k = u_{n+1}$

Table 1

k	$\beta_{0,k}$	$\beta_{1,k}$	$\beta_{2,k}$	$\beta_{3,k}$	$\beta_{4,k}$	$\beta_{5,k}$
0	b_1	0	a_1	a_2	0	0
1	b_2	0	0	a_3	a_4	0
2	d	0	0	0	c_1	c_2

at k=3, 4 and 5, etc., then the variables of the equation (2) and system (1) will be connected according to Table 2. This table easily to continue for k>3.

Table 2

k	w_k	v_{k-1}	v_{k-2}	v_{k-3}	v_{k-4}	v_{k-5}
0	u_n	y_{n-1}	x'_n	x''_n	y_{n-2}	x'_{n-1}
1	u_n	x''_{n+1}	y_{n-1}	x'_n	x''_n	y_{n-2}
2	u_n	x'_{n+1}	x''_{n+1}	y_{n-1}	x'_n	x''_n
3	u_{n+1}	y_n	x'_{n+1}	x''_{n+1}	y_{n-1}	x'_n

From Table 2 follows, that $v_{k-1} = y_{n-1}$ at k=0, $v_{k-1} = y_n$ at k=3, etc. Therefore the equation (2) can be used for realization of the system (1). The equation (2) in essence describes multiplex implementation of the considered section.

The distributed arithmetic state-space section appropriate to the equation (2) is shown on Fig.2a. It uses one ROM organized as 128 words on B bit and one accumulator instead of three as on Fig. 1b. Two uninvolved address of ROM are necessary for periodical choice of memory contents, appropriate to one of three sets of the coefficients from Table 1. Other realization variant of the state-space section is shown on Fig. 2b. The introduction of two switches result in ROM organized as 32 words on B bit. We shall notice that use of the additional logic circuits [3] in realizations on fig. 2a,b permits to reduce the number of words in ROM in two times. Because of multiplexing the proposed realizations of the state-

space section concede in speed of the realization on Fig. 1b (in three times) and require some complication of a control unit.

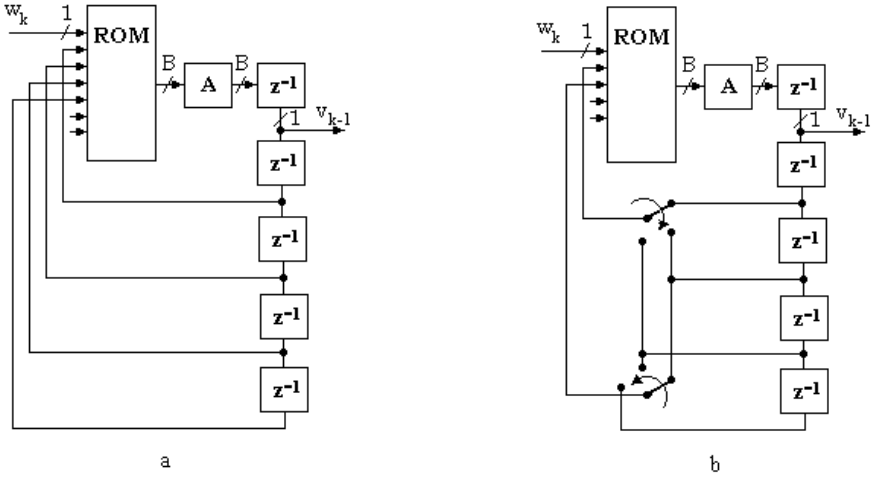

Fig.2. Distributed arithmetic state-space sections: a) without switches and b) with switches.

The distributed arithmetic state-space sections indicated here and in [2,3] differ in the memory size, number and organization of ROM's, the number of accumulators, delay elements and additional adders, complexity of a control unit and speed. The choice of that or other construction of the section will be defined by used element base, requirements to the particular project and more detailed development of the functional and basic circuits. The proposed realizations of the state-space section give additional degrees of freedom at designing of digital filters with distributed arithmetic on the basis of custom VLSI.

References

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